FACULTY OF ENGINEERING & TECHNOLOGY

Effective from Academic Batch: 2022-23

Programme: **BACHELOR OF TECHNOLOGY (Electronics and Communication)**

Semester: **VII**

Course Code: **202060704**

Course Title: **Advanced VLSI Design**

Course Group: Professional Elective Course

Course Objectives: Chip design is a computer aided design process in current scenario. This course provides a platform for students to understand importance of testing, fundamental VLSI test principles, basic concepts of design of testability (DFT), logic simulation and fault simulation, and various techniques for test pattern generation etc. To design chip now a day's industry prefers to test it carefully on computer aided software tools. The software tools support hardware descriptive language (HDL) compiler. The chip designer can able to program and test the programs on simulator. The front-end design can also, be tested on FPGA/CPLD development kits.

Teaching & Examination Scheme:

Contact hours per week			Course Credits	Examination Marks (Maximum / Passing)				
				Theory		J/V/P*		Total
Lecture	Tutorial	Practical		Internal	External	Internal	External	
3	0	2	4	50/18	50/17	25/9	25/9	150/53

* **J**: Jury; **V**: Viva; **P**: Practical

Detailed Syllabus:

Sr.	Contents	Hours
1	**Introduction:** Importance of Testing, Testing during VLSI Lifecycle, Challenges in VLSI Testing, Levels of Abstraction in VLSI Testing, Historical Review of VLSI Test Technology.	8
2	**Verification:** Importance of verification, Verification plan, Verification flow, Levels of verification, Verification methods and languages	8
3	**Functional Verification:** Introduction to test bench, Test bench architecture, Types of test benches, case study	12
4	**Introduction to Digital Design**: Introduction to hardware descriptive language (HDL). Difference between computer programming languages and HDLs Examples and HDL based digital design flow based on FPGA and CPLD.	5

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5	**Basic concepts of HDL** (Verilog/VHDL): Level of abstractions supported by HDLs, Data types and syntaxes of HDLs. Instantiation concepts. Switch level modeling and its example, Behavioral Level modeling, Structural modeling, Dataflow modeling.	**6**
6	**Hardware Modeling Examples**: ALU, Binary multiplier, Pulse counter, Barrel shifter, UART, Traffic light controller, DRAM Model, DFT, Testability, etc.	**6**
		45

List of Practicals / Tutorials:

1	Introduction to HDL language Verilog/VHDL
2	Implement basic digital logic gates and simulate with HDL.
3	Design and implement half adder logic with HDL and simulate the same.
4	Design and implement full adder logic with HDL and simulate the same.
5	Design and implement fast adder logic with HDL and simulate the same.
6	Design and implement multiplexers with HDL and simulate the same.
7	Design and implement multiplier with HDL and simulate the same.
8	Design and implement 4-bit counter with HDL and simulate the same.
9	Design the Mask layout of the Combinational circuits and simulate the same.
10	Design the complete mask layout for the Finite State Machine (FSM).
11	Design the complete mask layout for the 8-bit ALU.

Reference Books:

1	Wang Wu Wen, **VLSI Test Principles and Architectures**, Morgan Kaufmann Publishers.
2	M. Bushnell and V. D. Agrawal, **Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits**, Kluwer Academic Publishers, 2000
3	M. Abramovici, M. A. Breuer and A. D. Friedman, **Digital Systems Testing and Testable Design**, IEEE Press, 1990
4	T. Kropf Introduction to Formal Hardware Verification, , Springer Verlag, 2000
5	Janick Bergeron, Writing Testbenches, **Functional Verification of HDL Models**, Springer
6	P. Rashinkar, Paterson and L. Singh, **System-on-a-Chip Verification- Methodology and Techniques**, Kluwer Academic Publishers, 2001
7	**Circuit Design and Simulation with VHDL**, Volnei A. Pedroni.,The MIT Press, Cabridge,2010
8	**Verilog HDL A Guide to Digital Design and Synthesis**, Samir Palnitkar, Pearson Education.
9	**VHDL Primer**, J. Bhaskar, PHI.

Supplementary learning Material:	
1	www.xilinx.com, Xilinx project navigator evaluation tools version.
2	www.ocw.mit.edu , MIT Open Courseware
3	www.mosis.com A pioneer in Multi Project Wafer (MPW) fabrication services

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4	System Design Through VERILOG, IIT Guwahati: https://nptel.ac.in/courses/108103179
5	Digital System Design, IIT Ropar: https://onlinecourses.nptel.ac.in/noc21_ee39/preview

Pedagogy:

- Direct classroom teaching
- Audio Visual presentations/demonstrations
- Assignments/Quiz
- Continuous assessment
- Interactive methods
- Seminar/Poster Presentation
- Industrial/ Field visits
- Course Projects

Internal Evaluation:

The internal evaluation comprised of written exam (40% weightage) along with combination of various components such as Certification courses, Assignments, Mini Project, Simulation, Model making, Case study, Group activity, Seminar, Poster Presentation, Unit test, Quiz, Class Participation, Attendance, Achievements etc. where individual component weightage should not exceed 20%.

Suggested Specification table with Marks (Theory) (Revised Bloom's Taxonomy):

Distribution of Theory Marks in %						**R**: Remembering; **U**: Understanding; **A**: Applying; **N**: Analyzing; **E**: Evaluating; **C**: Creating
R	**U**	**A**	**N**	**E**	**C**	
10	**20**	**20**	**20**	**15**	**15**	

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Course Outcomes (CO):

Sr.	Course Outcome Statements	%weightage
CO-1	To realize importance and challenges of VLSI Testing at different abstraction levels.	**25**
CO-2	To identify the different characteristics of verification, and apply different verification methods.	**25**
CO-3	Work with Hardware Descriptive Language like Verilog/VHDL and various EDA tools used in chip design process.	**25**
CO-4	Implement various digital logic blocks on FPGA/CPLD boards.	**25**

Curriculum Revision:	
Version:	**2.0**
Drafted on (Month-Year):	June -2022
Last Reviewed on (Month-Year):	-
Next Review on (Month-Year):	June-2025

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